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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,845	12/22/2003	Vladislav Vashchenko	NSC1-M4400 [P05771]	9084

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,845	VASHCHENKO ET AL.	
	Examiner	Art Unit	
	Evan Pert	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-12 in the reply filed on December 23, 2004 is acknowledged. While applicant "does not necessarily agree with the need for restriction," applicant did not point out any errors in the restriction requirement. Accordingly, applicant's response, including cancellation of non-elected claims, is treated as an election without traverse (MPEP § 818.03(a)).

Specification

2. At page 5, lines 20-21, applicant writes: "The thin insulating layer of silicide can act as a thin insulating barrier in order to serve as a tunneling junction for spin-polarized carriers." Yet, a "silicide" is not "insulating" because a silicide is notoriously known as "conductive" having "low resistivity," as stated in other parts of applicant's specification. Furthermore, "tunneling" is a seemingly improper way to describe electrons (spin polarized or not) passing through a *conductive* silicide layer that seemingly should conduct electrons of any spin.

Appropriate correction or explanation is required.

Claim Objections

3. Claims 10 and 11 are objected to for being duplicates of each other.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. (US 6,753,562).

Regarding claim 1, the Hsu et al. reference discloses a system (e.g. Fig. 5) for injecting spin based electrons into silicon (i.e. substrate 101 can be "silicon" per col. 9, line 60), comprising: a ferromagnetic metal contact (106) capable of transmitting carriers having a primary spin polarization (i.e. "spin polarized conduction electrons" per col. 10, lines13-16); and a silicide layer (120) positioned between the ferromagnetic metal (106) contact and the silicon (101), the silicide layer making ohmic contact with the silicon such that the spin-polarized carriers transmitted from the ferromagnetic metal contact can be injected into the silicon without altering the primary spin polarization (i.e. the silicide is present making ohmic contact since "the Schottky barrier effect is eliminated or reduced," wherein, as implicitly disclosed by the Hsu et al. reference, the spin-polarized carriers transmitted from the source can be injected without altering the primary spin polarization [see col. 2, lines 52-66].)

Regarding claim 2, the Hsu et al. reference discloses the inclusion of a silicon Substrate (101), the silicide layer (120) being disposed on a surface of the silicon substrate (101) and acting as a tunneling junction between the ferromagnetic metal contact and the silicon substrate (wherein the "acting as a tunneling junction" limitation is anticipated since the electrons pass through the thin silicide).

Regarding claim 3, the Hsu et al. reference discloses that the ferromagnetic metal contact and silicide layer form a source electrode [e.g. "source" in Fig. 5].

Regarding claim 4, the Hsu et al. reference discloses a drain electrode contacting the silicon, the drain electrode [e.g. "drain" in Fig. 5] including a ferromagnetic detection contact (107) capable of receiving the spin-polarized carriers (injected from the "source"), and further including a second silicide layer ("not shown" per col. 11, line 17) disposed between the ferromagnetic detection contact (107) and the silicon substrate (101/103) such that the spin-polarized carriers flowing into the ferromagnetic detection contact from the silicon substrate maintain spin polarization (explanation of "spintronic device at col. 3, building on explanation of MRAM implementation at col. 2, lines 37-44).

Regarding claim 5, the Hsu et al. reference discloses a gate electrode positioned on the silicon substrate, the gate electrode capable of receiving a gate bias and applying an electric field across the silicon substrate such that spin-injected carriers flowing through the electric field tend to change spin orientation (wherein "Plate-O," "Gate," and "Plate-1" are reasonably all termed "gates" in that they are biased to apply electric fields that manipulate carriers flowing in a substrate below them as a "gate").

Regarding claim 6, the Hsu et al. reference discloses an external field generator capable of applying an electric field across the silicon such that spin-injected carriers flowing through the electric field tend to change spin orientation (such as the external field generator labeled "plate" in Fig. 4 per col. 10, lines 47-50).

Regarding claim 7, the Hsu et al. reference discloses a nanowire polygate (with 104 necessarily being a "nanowire" since it's on the order of nanometers per col. 7) positioned adjacent the silicon (separated by a gate insulator, like applicant) and capable of applying a magnetic field across the silicon such that spin-injected carriers flowing through the electric field tend to change spin orientation (wherein the "gate" in the reference is "capable" because it is depicted in a configuration indistinguishable from applicant's and wherein spin tends to "flipped" by gate voltage per page 6, lines 17-19).

Regarding claim 8, the Hsu et al. reference discloses the silicide layer is a cobalt silicide layer (col. 11, line 14).

Regarding claim 9, the Hsu et al. reference discloses the silicide layer is a nickel silicide layer (col. 11, line 15).

Regarding claims 10 and 11, the Hsu et al. reference discloses the ferromagnetic metal contact is a cobalt ferromagnetic metal contact (col. 8, lines 19-20).

Regarding claim 12, the Hsu et al. reference discloses a spin-based transistor (Fig. 5), comprising: a silicon substrate (101), a source electrode (i.e. "source") on the silicon substrate, the source electrode including a ferromagnetic injection contact (106) capable of injecting spin-polarized carriers into the silicon substrate (e.g. col. 2, lines 32-36), and further including a first silicide layer (120) disposed between the ferromagnetic injection contact (106) and the silicon substrate (101/102) such that carriers injected into the silicon substrate maintain spin polarization (discussion of "spintronic device" at col. 3 comapred to MRAM at col. 2); a drain electrode on the silicon substrate (e.g. "drain" in

Fig. 5), the drain electrode including a ferromagnetic detection contact (107) capable of receiving spin-polarized carriers (being "capable" because 107 acts as a "spin-analyzer ferromagnetic drain"), and further including a second silicide layer (not shown per col. 11, line 17) disposed between the ferromagnetic detection contact (107) and the silicon substrate (101/103) such that carriers flowing into the fenomagnetic detection contact from the silicon substrate maintain spin polarization (per the discussion of a "spin transistor" which is a "spintronic device" described at col. 3 as compared to an MRAM device at col. 2); and a gate electrode (104) positioned on the silicon substrate (101) between the source electrode and gate electrode (see Fig. 5), the gate electrode capable of receiving a gate bias (like any transistor "gate") and applying an electric field across the silicon substrate between the source and gate electrodes (a.k.a. the "channel") such that carriers flowing through the electric field will change spin orientation (wherein a voltage on the gate in the Hsu et al. reference will "tend to cause the spin-polarized electrons" to "flip" spin, per a universal fact stated at page 6, lines 17-19 of applicant's specification).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ETP
February 15, 2005

EVAN PERT
PRIMARY EXAMINER